COMPLETE LISTING OF CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) In a data communications receiver functionally connected to a communications loop to receive a data signal transmitted across the loop by a transmitter, the receiver having a linear equalizer operable to compensate for distortion in the data signal caused by the communications loop and a timing loop for maintaining signal timing between the transmitter and receiver, an improvement comprising a timing equalizer filter functionally positioned within the timing loop and ahead of the linear equalizer, the timing equalizer functionally independent from the linear equalizer whereby the signal timing controlled by the timing loop can be maintained independently of timing adjustments made in the linear equalizer.

2. (Currently Amended) The improved data communications receiver of claim 1 wherein the timing equalizer filter includes filter coefficients derived from ~~corresponding to~~ equalizer coefficients generated in the linear equalizer as a result of training of the linear equalizer.

3. (Original) The improved data communications receiver of claim 1 wherein the timing equalizer filter includes pre-determined filter coefficients based on use with a communications loop of moderate length.

4. (Original) The improved data communications receiver of claim 1 wherein the timing loop comprises an early-late timing loop having a phase detector with a

signal input functionally linked to an output of the timing equalizer filter, a loop filter functionally coupled to an error signal output of the phase detector, and a voltage controlled oscillator functionally positioned between the loop filter and the timing equalizer filter.

5. (Currently Amended) An improved method of acquiring and maintaining signal timing between a data communications transmitter and receiver connected at respective central and remote ends of a communications loop, where the receiver includes a timing loop and a linear equalizer operable to compensate for distortion of a received data signal caused by the communications loop, the improvement comprising the steps of:

a. setting filter coefficients in a timing equalizer filter that is functionally positioned in the timing loop; ~~and~~

b. passing the received data signal through the timing equalizer filter prior to inputting the received data signal to a phase detector portion of the timing loop; and

c. operating the timing equalizer filter in a data path separate from the linear equalizer.

6. (Original) The method of claim 5 wherein the step of setting the filter coefficients in the timing equalizer filter is performed by copying equalizer coefficients from the linear equalizer to the timing equalizer filter.

7. (Original) The method of claim 5 wherein the step of setting the filter coefficients in the timing equalizer filter is performed by entering filter coefficients

into the timing equalizer filter that are based on predetermined compromise equalizer coefficients corresponding to a communications loop having predicted signal distortion characteristics.

8. (Original) A method of time locking a receiver to a transmitter in a communications system that sends random digital data signals across a communications loop, where the receiver includes a linear equalizer having adjustable equalizer coefficients and an early-late timing loop adapted to acquire and maintain the time locking, the method comprising functionally positioning a timing equalizer filter in the timing loop and setting filter coefficients in the timing equalizer filter such that operation of the timing loop can proceed independent of subsequent adjustment of the linear equalizer.

9. (Original) The method of claim 8 wherein the filter coefficients are set in the timing equalizer filter by training the linear equalizer and then copying equalizer coefficients from the linear equalizer to the timing equalizer filter.

10. (Currently Amended) An improved method for acquiring timing in a data communications receiver having a received signal and a linear equalizer, the method comprising the steps of:

a. sampling the received signal to provide a sampled signal;

b. equalizing the sampled signal with a timing equalizer filter to provide an equalized signal, the timing equalizer filter functionally independent from the linear equalizer;

c. phase detecting the equalized signal to provide a phase error signal;

d. filtering the phase error signal with a loop filter thereby providing a control voltage; and

e. adjusting a voltage controlled oscillator in response to the control voltage whereby the output of the voltage controlled oscillator provides timing for the data communications receiver.

11. (Currently Amended) An apparatus for acquiring timing in a data communications receiver having a received signal and a linear equalizer, the apparatus comprising:

a. a timing equalizer filter functionally coupled to the received signal to provide an equalized signal;

b. a phase detector functionally coupled to the timing equalizer filter and operable to detect a phase difference in the equalized signal and to provide a responsive phase error signal; ~~and~~

c. a loop filter and a voltage-controlled oscillator functionally arranged to generate a timing signal in response to the phase error signal; and

d. the timing equalizer filter, phase detector, loop filter and voltage controlled oscillator defining a timing loop path independent from the linear equalizer.

12. (Currently Amended) A data communications receiver for receiving a stream of user data transmitted from a transmitter across a communications loop comprising:

a. a demodulator adapted to receive and process the user data;

b. a linear equalizer operably coupled to receive and equalize the output from the demodulator;

c. a timing loop operable to generate a timing signal to time lock the receiver to the transmitter using timing information derived from the stream of user data; and

d. a timing equalizer filter functionally positioned independently of the linear equalizer to receive and process data from the demodulator to provide an equalized signal to the timing loop.